REMARKS

Applicant has studied the Office Action dated April 14, 2004 and has made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-26 are pending. Claims 1-3, 5, 6, 10-14, and 18-22 have been amended, and new claims 25 and 26 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

The Examiner requested corrected formal drawings in which Figures 1a, 1b, 2, and 3 were designated by a legend such as "Prior Art". Applicant is in the process of obtaining corrected formal drawings that incorporate the changes requested by the Examiner, and will forward them to the Examiner as soon as they are available.

The abstract of the disclosure was objected to because the length exceeds 150 words. The abstract has been amended so as to not exceed 150 words. No new matter has been added. It is submitted that the abstract now fulfills the requirements of MPEP § 608.01. Therefore, it is respectfully submitted that the objection to the abstract should be withdrawn.

Claims 1-7, 10-15, and 18-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chren, Jr. (U.S. Patent No. 5,430,764) in view of Arkin (U.S. Patent No. 5,917,834). Claims 8, 9, 16, 17, 23, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chren, Jr. in view of Applicant's Admitted Prior Art ("AAPA"). These rejections are respectfully traversed.

The present invention is directed to Residue Number System (RNS) arithmetic circuits that have simple circuitry for performing built-in self testing of the input-to-output (i.e., propagation) delay of the circuit. One embodiment of the present invention provides an arithmetic circuit with built-in self testing of input-to-output delay for use with an RNS. The

arithmetic circuit includes an arithmetic core for performing an RNS arithmetic operation, input-to-output delay test circuitry coupled to the arithmetic core, and input-to-output delay logic circuitry coupled to the output of the arithmetic core.

The input-to-output delay test circuitry selectively feeds the output of the arithmetic core back to at least one of the inputs without latching so as to induce natural oscillation at the output of the arithmetic core during testing of the input-to-output delay. The input-to-output delay logic circuitry measures an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, makes a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value, and produces a pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification.

Because natural oscillation is induced at the output of the arithmetic core during testing by feeding back the output without latching, simple logic circuitry can be used to measure the frequency of this oscillation and determine whether or not the input-to-output delay of the arithmetic core is acceptable. Thus, the present invention provides simple and efficient built-in self test circuitry for the input-to-output (i.e., propagation) delay so that the RNS arithmetic circuits can be used in practical digital signal processing devices.

The Chren reference discloses digital frequency synthesizers that employ RNS-based processors to generate output waveforms. The Arkin reference discloses an integrated circuit tester having multiple period generators. However, neither Chren nor Arkin, or a combination of the two, discloses an RNS arithmetic circuit with built-in self testing of input-to-output delay that includes input-to-output delay test circuitry that selectively feeds the output of an arithmetic core back to at least one of the inputs without latching so as to induce natural oscillation at the output of the arithmetic core during testing of the input-to-output delay, and input-to-output delay logic circuitry that measures an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, makes a determination of whether this oscillation frequency is at least equal to a minimum threshold value, and produces a pass signal or a fail signal based on the determination in order to indicate whether or not the input-to-output delay of the arithmetic core

is within specification, as is recited in amended claim 1. Amended claim 10 contains similar recitations.

Similarly, neither Chren nor Arkin, or a combination of the two, discloses a method for testing propagation delay of an RNS arithmetic circuit in which the output of an arithmetic core is selectively fed back to one of the inputs without latching and a constant is selectively provided to another input of the arithmetic core so as to induce natural oscillation at the output of the arithmetic core during testing of the propagation delay, an oscillation frequency of the output of the arithmetic core is measured during testing of the propagation delay, a determination is made of whether this oscillation frequency is at least equal to a minimum threshold value, and a pass signal or a fail signal is produced based on the determination in order to indicate whether or not the propagation delay of the arithmetic core is within specification, as is recited in amended claim 18.

Chren discloses a digital frequency synthesizer that uses RNS arithmetic processors in the phase accumulator. As shown in Figure 3, the phase accumulator 120 has seven arithmetic units 121 that are each an RNS binary adder. The output of each RNS adder 121 is stored in a latch 122 under the control of the system clock f_c. The output of each RNS arithmetic unit 121 is stored in the latch 122 every clock cycle, and fed back as one of the inputs to that same RNS arithmetic unit 121 in the next clock cycle. The output of the phase accumulator 120, after being processed by a scalar circuit 127 and an address translator 126, is supplied as the read address to a dual port ROM 130 that stores samples of a sine wave to be generated. The output of the ROM 130 is coupled to a digital-to-analog converter 140 that produces the output sine wave signal V_o corresponding to the input data. Thus, the digital frequency synthesizer of Chren includes a phase accumulator having RNS adders that operate with feedback under control of the system clock. In other words, Chren teaches an accumulator that operates in a synchronous manner using clocked latching on the feedback path.

Arkin discloses an integrated circuit tester 10 that is connected between a host computer 24 and an integrated circuit 12 that is being tested, as shown in Figure 1. The tester 10 includes a

pattern generator 22 that receives test data from the host computer 24, and a channel CH(n) for each pin of the integrated circuit 12 being tested. Based on the received test data, the pattern generator 22 generates control signals for each of the channels CH(n) so as to produce a desired pattern of input signals on the input pins at specified timings during the testing. More specifically, each control signal from the pattern generator 22 is passed through timing circuitry, logic circuitry, and driving circuitry of one of the channels CH(n) in order to deliver a high or low logic level to the corresponding input pin of the integrated circuit 12 at a specific timing.

The timing circuits in each channel CH(n) include edge generators 40 and 44. As shown in Figure 2, each edge generator includes a multiplexer 50, a register 52, a counter 54, adders 58 and 60, and a delay circuit 56. The edge generator 40 controls the exact timing that the edge of the input data received from the pattern generator 22 is received at the input pin of the integrated circuit 12 based on a master clock signal MCLK, master and auxiliary period signals BOC and CVRN, and a calibration signal CAL. Additionally, each of the channels CH(n) includes logic circuitry for comparing the logic levels received from output pins of the integrated circuit 12 to the expected output logic levels for the input signals that are supplied by the pattern generator. If the logic level output from the output pin of the integrated circuit 12 does not match the excepted output logic level, a fail signal is output. Thus, the integrated circuit tester of Arkin supplies a predetermined pattern of input signals at specified timings to the input pins of the circuit being tested under control of a master clock signal, and determines if the resulting output logic levels of the circuit being tested are proper for the input signal pattern that was supplied.

The Examiner has taken the position that the combination of Chren and Arkin teaches all of the claimed features of the present invention, and that it is proper to combine the teachings of the Chren and Arkin references to produce such a combination. These positions of the Examiner are respectfully traversed.

First, embodiments of the present invention are directed to circuits and methods that measure the oscillation frequency at the output of the arithmetic core, and then determine and indicate whether or not the input-to-output (or propagation) delay of the arithmetic core is within

specification. Amended claims 1 and 10 recite "input-to-output delay logic circuitry measuring an oscillation frequency of the output of the arithmetic core . . . , making a determination of whether the oscillation frequency . . . is at least equal to a minimum threshold value, and producing a pass signal or a fail signal . . . to indicate whether or not the input-to-output delay of the arithmetic core is within specification." Similarly, amended claim 18 recites the steps of "measuring an oscillation frequency of the output of the arithmetic core . . . , making a determination of whether the oscillation frequency . . . is at least equal to a minimum threshold value, and producing a pass signal or a fail signal . . . to indicate whether or not the propagation delay of the arithmetic core is within specification." Thus, embodiments of the present invention determine whether an arithmetic circuit's input-to-output delay is acceptable based on the oscillation frequency at the output of the circuit.

Neither Chren nor Arkin ever mentions measuring an oscillation frequency of the circuit. In fact, neither Chren nor Arkin teaches or suggests causing the circuit to oscillate. Thus, neither Chren nor Arkin can possibly disclose either determining whether a measured oscillation frequency is at least equal to a minimum threshold value, or producing a pass signal or a fail signal based on such a determination.

While Arkin does disclose some logic circuitry that outputs a pass or fail signal, this logic circuitry monitors the logic level output from an output pin of the circuit being tested and outputs a pass or fail signal based on whether or not the output logic level matches the excepted output logic level for the pattern of input signals that was supplied to the circuit by the pattern generator. This is completely different than input-to-output delay logic circuitry that produces a pass or fail signal based on a determination about the oscillation frequency of the output of the circuit in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification. Furthermore, Arkin surely does not teach or suggest logic circuitry that measures the oscillation frequency of the output of the circuit being tested, and determines whether the measured oscillation frequency is at least equal to a minimum threshold value.

Applicant submits that the recited limitation of "measuring an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold

value, and producing a pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification" is not merely language of intended use. While the structure of some elements can be defined by a simple element name, other elements may not have such a convenient name and must be defined in a different manner. For example, a "comparator circuit" by definition has two inputs and is composed of basic circuit elements that create an output signal based on the relative levels of the input signals. On the other hand, many generically named (or defined) circuits such as "logic circuits" and "control circuits" do not define a set structure and must be more specifically described in order to define a specific structure.

In the present case, the recited element is an "input-to-output delay logic circuitry measuring an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value, and producing a pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification." This specific language is meant to define the structure of the input-to-output delay logic circuitry, not to recite an intended use of the claimed circuitry. In other words, this entire claim limitation is the name (or definition) of the element that is necessary to convey its structure.

Applicant's invention does not reside in what basic circuit elements are used to form the recited "input-to-output delay logic circuitry"; it can be formed by any combination of basic circuit elements that allow it to measuring an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value, and producing a pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification. Thus, Applicant submits that the recited "input-to-output delay logic circuitry" element must be considered as a structural limitation, and that the Examiner cannot disregard part of the definition of the input-to-output delay logic circuitry as being merely functional language or an intended

use. Further, amended claim 18 is a method claim, so the recited functional language cannot possibly be disregarded in this claim.

Neither Chren nor Arkin teaches or suggests a circuit or method that measures the oscillation frequency at the output of the arithmetic core, and then determines and indicates whether or not the input-to-output (or propagation) delay of the arithmetic core is within specification. This claimed feature of the present invention allows testing of the input-to-output (i.e., propagation) delay of RNS arithmetic circuits so that RNS arithmetic circuits can be used in practical digital signal processing devices.

Second, embodiments of the present invention are directed to circuits and methods that allow testing of the input-to-output delay of an arithmetic circuit (also known as the propagation delay). Amended claims 1 and 10 recite an "arithmetic circuit with built-in self testing of input-to-output delay", and amended claim 18 recites a "method for testing propagation delay of a Residue Number System (RNS) arithmetic circuit." Additionally, amended claims 1 and 10 recite functionality "during testing of the input-to-output delay" and producing a signal "to indicate whether or not the input-to-output delay of the arithmetic core is within specification." Similarly, amended claim 18 recites functionality "during testing of the propagation delay" and producing a signal "to indicate whether or not the propagation delay of the arithmetic core is within specification." Amended claims 1 and 10 also recite that the arithmetic circuit includes the elements of "input-to-output delay test circuitry" and "input-to-output delay logic circuitry". Thus, it is abundantly clear that the present invention is directed to testing an arithmetic circuit's input-to-output delay (i.e., the time it takes for a signal to propagate from the input to the output of the arithmetic circuit).

Chren never mentions any type of circuit testing, and never even suggests that circuit testing should or could be performed.

Arkin does disclose a circuit tester, but Arkin fails to teach a circuit or method for testing the input-to-output delay of an arithmetic circuit. The circuit tester of Arkin performs a test of the output states (or output logic levels) of the circuit. As explained above, Arkin teaches using a pattern generator to supply a certain pattern of input signals to the input pins at certain times, and

monitoring the output pins to determine whether the output signals from the circuit being tested match the expected logic states for the pattern of input signals that was supplied to the circuit by the pattern generator. See Arkin at 3:16-26. Thus, Arkin teaches a circuit tester that performs state (or logic level) testing based on an input signal pattern, and fails to teach or suggest input-to-output delay testing.

The Examiner has taken the position that testing of the input-to-output delay of a circuit is taught by the edge generators in the circuit tester of Arkin. The edge generators of Arkin include a "delay circuit" for delaying an input signal being supplied to the circuit being tested for a portion of the master clock period in order to allow the input signal to be supplied at a specific timing. While the "delay circuit" of Arkin does delay the time that an input signal is supplied to the circuit being tested, this is completely different than testing the input-to-output delay of the circuit being tested. Applicant fails to understand how using a "delay circuit" to delay an input signal to the circuit being tested even has any relevance to testing of the input-to-output delay of the circuit.

Furthermore, amended claims 1 and 10 recite a "circuit with built-in self testing". The circuit tester of Arkin is a complex stand-alone device that is connected between a host computer and the integrated circuit being tested. This is completely different from the embodiments of the present invention recited in amended claims 1 and 10, which are directed to arithmetic circuits having simple built-in circuitry for performing a self-test of circuit.

Neither Chren nor Arkin teaches or suggests a circuit or method that allows testing of the input-to-output delay of an arithmetic circuit. This claimed feature of the present invention allows testing of the input-to-output (i.e., propagation) delay of RNS arithmetic circuits so that RNS arithmetic circuits can be used in practical digital signal processing devices.

Third, in embodiments of the present invention, the output of the arithmetic core is selectively fed back to an input without latching so as to induce natural oscillation at the output of the arithmetic core. Amended claims 1 and 10 recite "input-to-output delay test circuitry selectively feeding the output of the arithmetic core back to at least one of the inputs without latching so as to induce natural oscillation at the output of the arithmetic core during testing of

the input-to-output delay." Similarly, amended claim 18 recites the step of "selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching . . . so as to induce natural oscillation at the output of the arithmetic core during testing of the propagation delay." Thus, embodiments of the present invention test of the input-to-output delay of the circuit by feeding back the output of the circuit to an input without latching so as to induce natural oscillation at the output.

Arkin only teaches providing a pattern of input signals to the inputs of the circuit being tested and monitoring the resulting states of its outputs. Arkin never mentions providing any output-to-input feedback for the circuit being tested. Additionally, Arkin requires use of latching and a master clock signal along with other timing signals during testing so that the tester supplies the input signals to the circuit being tested at specific timings in a synchronous manner.

Chren does disclose RNS arithmetic circuit whose outputs are fed back to inputs, but Chren fails to teach feeding back the output of an arithmetic circuit to an input without latching so as to induce natural oscillation at the output of the circuit. As explained above, in Chren, the output of each RNS arithmetic unit is stored in a latch every clock cycle under the control of the system clock. The value stored in the latch is then fed back as one of the inputs to the arithmetic unit in the next clock cycle. Thus, Chren teaches using clocked latching on the feedback path so as to produce an RNS arithmetic unit that operates in a synchronous manner under control of the system clock.

While Chren teaches a synchronous arithmetic circuit that uses clocked latching on the feedback path, embodiments of the present invention do not using any latching or clock control of the feedback path. In the present invention, during input-to-output delay testing, latching is not present on the feedback path so the arithmetic circuit oscillates naturally. See specification at 12:3-12; Figs. 5 and 6. In other words, the arithmetic circuit oscillates non-stop by its very nature without any external signals or control. Further, the period of this natural oscillation is directly proportional to the quantity being tested -- the input-to-output delay. This allows simple circuitry to be used to more accurately test the input-to-output delay of the circuit.

For example, in some embodiments of the present invention a counter is used to determine the oscillation frequency from multiple input-to-output passes (natural oscillations) of

the signal. Chren teaches an arithmetic circuit that operates in a synchronous manner using latching on the feedback path, so the oscillation frequency of the arithmetic circuit of Chren will always be the same as the clock frequency. Natural oscillation is not possible in the arithmetic circuit of Chren due to this latching on the feedback path, so the natural oscillation frequency cannot be measured and then used to test the input-to-output delay of the circuit. Testing the input-to-output delay of the arithmetic circuits of Chren requires the use of much more complex circuitry and external clock signals to set up a precise timing window for testing the time for one input-to-output pass of the signal. Furthermore, Chren never mentions any type of circuit testing, so the reference cannot possibly teach feeding the output back to the input without latching so as to induce natural oscillation during testing of the input-to-output delay.

Neither Chren nor Arkin teaches or suggests a circuit or method in which the output of a circuit is fed back to an input without latching during testing of the input-to-output delay. By providing a feedback path without latching or synchronous control, this claimed feature of the present invention induces natural oscillation at the output of the circuit, which allows simple circuitry to be used to accurately test the input-to-output delay of the circuit.

Applicant believes that the differences between Chren, Arkin, and the present invention are clear in amended claims 1, 10, and 18, which set forth various embodiments of the present invention. Therefore, claims 1, 10, and 18 distinguish over the Chren and Arkin references, and the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

As discussed above, claims 1, 10, and 18 distinguish over the Chren and Arkin references. Furthermore, the claimed features of the present invention are not realized even if the teachings of the AAPA are incorporated into Chren and Arkin. The AAPA does not teach or suggest the claimed features of the present invention that are absent from Chren and. Thus, claims 1, 10, and 18 distinguish over Chren, Arkin, and the AAPA, and thus, claims 2-9, claims 11-17, and claims 19-24 (which depend from claims 1, 10, and 18, respectively) also distinguish over Chren, Arkin, and the AAPA.

Furthermore, Applicants submit that limitations in the dependent claims are absent from the Chren and Arkin references. For example, dependent claim 2 recites that the input-to-output delay logic circuitry includes a counter that counts oscillations of the output of the arithmetic core during testing of the input-to-output delay, and a comparator that compares the output of the counter after a predetermined test period with the minimum threshold value and producing the pass or fail signal. Neither Chren nor Arkin teaches or suggests input-to-output delay logic circuitry that includes such a counter and comparator. Additionally, dependent claim 3 recites that the input-to-output delay test circuitry includes isolation buffers for isolating the inputs of the arithmetic core from upstream circuitry and the output of the arithmetic core from downstream circuitry during testing of the input-to-output delay, and at least one transmission gate for feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching during testing of the input-to-output delay. Neither Chren nor Arkin teaches or suggests input-to-output delay test circuitry that includes such a transmission gate and isolation buffers. Therefore, it is respectfully submitted that the rejection of claims 1, 8-10, 16-18, 23, and 24 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 25 and 26 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 25 and 26 are allowable for at least the reasons set forth above with respect to claims 1-24.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

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